

REMARKS/ARGUMENTS

The claims have been amended to clarify the invention recited therein. Claim 26 has been cancelled from the application. Claims 1-25 are pending in the application.

The rejections raised in the Office Action are addressed as follows.

Double Patenting re U.S. Patent No. 6,683,928

The Examiner rejected claims 1-9, 13-21, 25 and 26 as being unpatentable over claims 1-3 of U.S. Patent No. 6,683,928 on the ground of nonstatutory obviousness-type double patenting. Applicant respectfully disagrees for the reasons outlined below.

Claim 1 of U.S. Patent No. 6,683,928 is directed to a delay compensation circuit consisting of a system clock input, a first path having controllable fine delay elements, a second path having a coarse delay element, a phase detector and a counter. The first and second paths receive a system clock from the system clock input for providing delayed clock signals to the phase detector. The output of the phase detector is then used by the counter to provide an output for adjusting the number of fine delay elements in the first path.

Claim 1 of the present application is directed to a circuit for modeling a coarse delay element, having first and second delay paths, a phase detector, a counter and a decoder. The first and second delay paths receive and delay a clock signal. The phase detector detects a phase difference between the delayed clock signal received from the first and second delay paths and provides the phase difference to a counter. An output of the counter is then used by a decoder, which adjusts the delay provided by the first delay path.

Claim 1 of the present application recites a feature absent in claims 1-3 of U.S. Patent No. 6,683,928, namely the decoder element. Therefore, the Examiner's double patenting rejection to claims 1-9 of the present application is improper as claim 1 of U.S. Patent No. 6,683,928 would not anticipate nor render obvious, claim 1 of the present application. Withdrawal of the Examiner's double patenting rejection to claims 1-9 is respectfully requested.

Claims 13 and 25 of the present application have been amended to clarify that all the delay elements of the first delay path and the second delay path are active for delaying the receive clock signal to provide first and second clock delay signals. In otherwords, every delay element is used for providing the delayed clock signals.

Claim 1 of U.S. Patent No. 6,683,928 specifically states that the counter provides an output result "*for adjusting the number of fine delay elements in the first path*". Therefore, by adjusting the number of fine delay elements in the first path, a desired delay of the clock signal can be obtained. Claims 13 and 25 of the present application adjusts the delay of the first delay path while all the delay elements of the first delay path are active. This should be understood to mean that each delay element will provide an intrinsic delay inherent to the circuit, or a further delay. Therefore, the Examiner's double patenting rejection to claims 13-21 and 25 of the present application is believed to be overcome in view of the aforementioned amendments to claims 13 and 25 and arguments. Withdrawal of the Examiner's double patenting rejection to claims 13-21, 25 and 26 is respectfully requested.

Double Patenting re U.S. Patent No. 6,327,318

The Examiner rejected claims 1- 26 as being unpatentable over claim 1 of U.S. Patent No. 6,327,318 on the ground of nonstatutory obviousness-type double patenting. Applicant respectfully disagrees for the reasons outlined below.

Claim 1 of U.S. Patent No. 6,327,318 is directed to a delay compensation circuit having a coarse delay element, an adjustable fine delay, a counter, a circuit for applying a representation of the system clock and a circuit for applying a fine delay count. Claim 1 of U.S. Patent No. 6,327,318 states that the number of fine delay elements required to provide a delay which is equal to that of the second delay path is determined.

As previously discussed, claim 1 of the present application recites a decoder for adjusting the delay provided by the first delay path in response to a signal from the counter. Therefore, claim 1 of the present application recites a feature absent in claim 1 of U.S. Patent No. 6,683,928, namely the decoder element. Therefore, the Examiner's double patenting rejection to claim 1 of the present application is improper as claim 1 of U.S. Patent No. 6,683,928 would not anticipate nor render obvious, claim 1 of the present application.

As previously mentioned, claims 13 and 25 of the present application have been amended to clarify that all the delay elements of the first delay path and the second delay path are active for delaying the receive clock signal to provide first and second clock delay signals. Claim 1 of U.S. Patent No. 6,683,928 recites that a number of fine delay elements providing a delay equal to the second delay path is determined. The invention of claims 13 and 25 on the other hand, recite that all the delay elements remain active and are in use for delaying the

clock signal in response to the control signal from the counter. This should be understood to mean that each delay element will provide an intrinsic delay inherent to the circuit, or a further delay. Therefore, the Examiner's double patenting rejection to claims 1-26 of the present application is believed to be overcome in view of the aforementioned amendments to claims 13 and 25 and arguments. Withdrawal of the Examiner's double patenting rejection to claims 13-21, 25 and 26 is respectfully requested.

Claim rejections under 35 U.S.C. 102(b)

The Examiner rejected claims 1-9, 13-21, 25 and 26 as being anticipated by U.S. Patent No. 5,515,403 (Sloan et al.). Applicant respectfully disagrees, and submits that Sloan et al. does not teach an element recited in claims 1, 13 and 25. Applicant traverses the Examiner's rejection as follows.

Independent claims 1, 13 and 25 each recite that all of the delay elements of the first delay path and the second delay path remain active for delaying the clock signal they each respectively receive to provide first and second clock delay signals. By example, the embodiment of the invention shown in Figure 5 shows two delay elements 31A and 31B of a first delay path that are always active for delaying the clock signal DIV_CLK. Paragraph [0040] of the present application states "*The fine delay elements 39A and 39B have their control inputs set to 0, so that the path through them includes only their intrinsic delay.*". Therefore, no delay element of this delay path is ever bypassed or disabled for generating the delayed output clock signal. All the delay elements will be in use for generating the delayed output clock signal.

In contrast, the system of Sloan et. al. will have delay elements that are not used for generating the delayed output clock signal. Figure 8 of Sloan et al. is a block diagram of a circuit having one delay path consisting of coarse delay stage 192 and a fine delay stage consisting of coarse delay stage 194 and fine delay stage 196. Sloan et al. states at column 6, lines 44-47 that "*Fine delay stage 196 also includes an array of delay elements (not shown), coupled in a similar manner as medium delay stage 112 in FIG. 6.*", where Figure 6 shows delay stage 112 as a string of delay elements 140-146 with signal taps between each delay element and a multiplexor 148. Figure 9 illustrates an implementation of coarse delay stage 192 and 194, with a string of delay elements 202-208 with signal taps between each delay element and multiplexors 210 and 212. The configuration of coarse delay stage 192 is virtually

identical to that of delay stage 112, which is described by Sloan et al. as being an implementation of the fine delay stage. In both examples, the delayed output clock signal is provided at the output of the multiplexors as this is the signal being used by the subsequent circuits.

In operation, the Sloan et al. fine and coarse delay stages will bypass one or more delay elements depending on the input to be passed by the multiplexor. Figure 16 of Sloan et al. describes the method of operating the circuit of Figure 8, which includes adding a value of 1 to the multiplexor input signal. This has the effect of selecting the next subsequent input corresponding to the output of the next subsequent delay element in the string of delay elements. Therefore, one or more delay elements will not be active for delaying the clock signal. In Figure 9 for example, having multiplexor 210 selecting input 3 to pass to its output will pass the output signal from delay element 204 to the output of multiplexor 210 as the delayed output clock signal. The remaining downstream delay elements serve no purpose and are effectively inactive for providing the delayed output clock signal since their outputs are prevented from being passed to the multiplexor output. It is noted that multiplexor 212 receives the same input signal as multiplexor 192, thereby it passes the same output signal from delay element 204 to its output.

Applicant submits that Sloan et al. does not disclose or teach a delay system having all delay elements of the first delay path and the second delay path being active for delaying the clock signal to provide first and second clock delay signals, as recited in independent claims 1, 13 and 25. Therefore, claims 1, 13 and 25 are not anticipated by Sloan et al., and claims 2-9, and 14-21 which depend either directly or indirectly from claims 1 and 13 are not anticipated by Sloan et al. Withdrawal of the Examiner's rejection to claims 1-9, 13-21, 25 and 26 under 35 U.S.C. 102(b) is respectfully requested.

Applicant takes the opportunity to argue that claim 1 is not anticipated by Sloan et al. on other grounds. Claim 1 recites a counter for receiving a phase difference from a phase detector, and a decoder for receiving a signal from the counter. The phase detector detects a phase difference between delayed output clock signals from the first and second delay paths. The decoder is connected to the delay elements of one delay path for adjusting the delay therein. It should be clear to those skilled in the art that the previously recited elements of claim 1 describes a feedback loop configuration.

The Examiner equates the recited counter and decoder to the microprocessor described at column 6, lines 38-49. Respectfully, nowhere does Sloan et al. describe or infer that the microprocessor executes counter and decoder functionality analogous to those recited in claim 1. While feedback control using the microprocessor may be inferred, Sloan et al. does not teach or disclose that it is done using a counter and a decoder as recited in claim 1 of the present application.

Applicant therefore submits that claim 1, and claims 2-9 which depend directly or indirectly from claim 1, are not anticipated by Sloan et al. Withdrawal of the Examiner's rejection to claims 1-9 under 35 U.S.C. 102(b) is further requested.

Should the Examiner wish to discuss the Applicant's argument or claim amendments, he is invited to contact Shin Hung at 613-787-3571.

The Commissioner is hereby authorized to debit \$120.00 from Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP, representing the fee for a one month extension of time.

The Commissioner is hereby authorized to charge any additional fees, and credit any over payments to Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP.

Respectfully submitted,

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